METHOD AND STRUCTURE OF A DISPOSABLE REVERSED SPACER PROCESS FOR HIGH PERFORMANCE RECESSED CHANNEL CMOS

ABSTRACT OF THE INVENTION

A high-performance recessed channel CMOS device including an SOI layer having a recessed channel region and adjoining extension implant regions and optional halo implant regions; and at least one gate region present atop the SOI layer and a method for fabricating the same are provided. The adjoining extension and optional halo implant regions have an abrupt lateral profile and are located beneath said gate region.